PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Singh et al.	Group Art Unit: Unassigned
	Examiner: Unassigned
Application No. 10/633,021	
Filed: 7/31/2003	Atty. Docket No. NVIDP235/ P000846
For: PAD OVER ACTIVE CIRCUIT SYSTEM AND METHOD WITH FRAME SUPPORT STRUCTURE	Date: November 6, 2003

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450 on November 6, 2003.

Signed: Erica L. Farlow

Erica L. Farlow

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §§1.56 AND 1.97(b)

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§ 1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is believed to be filed before the mailing date of a first Office Action on the merits. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 50-1351 (Order No. NVIDP235/P000846).

Respectfully submitted,
Silicon Valley IP Group, PC

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Form 1449 (Modified)	Atty. Docket No. NVIDP235/P000846	Application No.: 10/633,021
Information Disclosure Statement By Applicant	Applicant: Singh et al.	
(Use Several Sheets if Necessary)	Filing Date: 7/31/2003	Group Art Unit: Unassigned

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,538,326	03/25/2003	Shimizu et al.	257	758	10/4/2001
	B	6,552,438	04/22/2003	Lee et al.	257	784	12/21/2000
	C	5,965,903	10/12/1999	Chittipeddi et al.	257	48	02/12/1998
	D	6,297,562	10/02/2001	Tilly	257	780	09/20/1999
	E	6,232,662	05/15/2001	Saran	257	750	07/02/1999
	F	6,365,970	04/02/2002	Tsai et al.	257	751	12/10/1999
	G	6,417,087	07/09/2002	Chittipeddi et al.	438	612	12/16/1999
	H	4,636,832	01/13/1987	Abe et al.	357	68	03/04/1986
	I	4,723,197	02/02/1988	Takiar et al.	361	403	12/16/1985
	J	6,100,589	08/08/2000	Tanaka	257	758	08/19/1997
	K	4,984,061	01/08/1991	Matsumoto	357	68	05/10/1988
	L	6,384,486	05/07/2002	Zuniga et al.	257	781	12/10/1999
	M	6,400,026	06/04/2002	Andou et al.	257	771	06/26/2000
	N	6,489,228	12/03/2002	Vigna et al.	438	612	10/02/2000
	O	6,358,831	03/19/2002	Liu et al.	438	612	03/03/1999
	P	5,965,903	10/12/1999	Chittipeddi et al.	257	48	02/12/1998
	Q	6,037,668	03/14/2000	Cave et al.	257	784	11/13/1998
	R	6,313,537	11/06/2001	Lee et al.	257	758	11/09/1998
	S	5,773,899	06/30/1998	Zambrano	257	784	08/29/1996
	T	6,144,100	11/07/2000	Shen et al.	257	762	10/28/1997
	U	5,751,065	05/12/1998	Chittipeddi et al.	257	758	10/30/1995

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	V	Heinen, Gail et al., "Wire Bonds Over Active Circuits", 1994, IEEE
	W *	Chou, Kuo-Yu et al., "Active Circuits Under Wire Bonding I/O Pads in 0.13 μm Eight-Level Cu Metal, FSG Low-K Inter-Metal Dielectric CMOS Technology +", October 2001, IEEE
	X *	Efland, T., et al., "LeadFrameOnChip offers Integrated Power Bus and Bond over Active Circuit", 2001, International Symposium on Power Semiconductor Devices & ICs, Osaka

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449 (Modified)	Atty. Docket No. NVIDP235/P000846	Application No.: 10/633,021
Information Disclosure Statement By Applicant	Applicant: Singh et al.	
(Use Several Sheets if Necessary)	Filing Date: 7/31/2003	Group Art Unit: Unassigned

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	Y	6,448,641	09/10/2002	Ker et al.	257	700	06/09/1999
	Z	6,486,051	11/26/2002	Sabin et al.	438	612	03/17/1999
	AA	6,489,688	12/03/2002	Baumann et al.	257	786	05/02/2001
	BB	6,087,732	07/11/2000	Chittipeddi et al.	257	786	09/28/1998
	CC	5,027,188	06/25/1991	Owada et al.	357	68	09/13/1989
	DD	6,329,712	12/11/2001	Akram et al.	257	700	03/25/1998
	EE	5,986,343	11/16/1999	Chittipeddi et al.	257	758	05/04/1998
	FF	6,016,000	01/18/2000	Moslehi	257	522	04/22/1998
	GG						
	HH						
	II						
	JJ						
	KK						
	LL						
	MM						
	NN						
	OO						
	PP						
	QQ						
	RR						
	SS						

The PTO did not receive the following listed Item(s)

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	TT	Saran, Mukul et al., "Elimination of Bond-pad Damage Through Structural Reinforcement of Intermetal Dielectrics", 1998, IEEE 36th Annual International Reliability Physics Symposium, Reno, Nevada

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.